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Development of Energy-Efficient Analog Front-End Circuits for Wearable Health Monitoring

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Abstract

Wearable health monitoring devices have become a cornerstone in preventive healthcare, enabling continuous physiological signal acquisition and real-time data analysis. However, the energy demands of these devices, particularly in the analog front-end (AFE) circuits, pose significant challenges for battery-powered operation. This study presents the design and optimization of an energy-efficient AFE for wearable health monitoring applications. The proposed design incorporates low-power operational transconductance amplifiers (OTAs), chopper-stabilized amplifiers for noise suppression, and optimized biasing strategies to reduce quiescent current consumption. Simulation results demonstrate a 35% reduction in power usage compared to conventional AFE architectures, achieving a total consumption of 42 μW while maintaining high signal fidelity with a signal-to-noise ratio (SNR) of 82 dB. The validation of the design was done by simulation in Cadence Virtuoso with standard CMOS 180 nm technology parameter. It has been estimated that a 100 mAh, 3.7 V battery will last for 5692.3 hours (237.2 days) with a 55x increase to 8809.5 hours (367.1 days), given no battery-life, use, or performance degradation. The results explain the proposed architecture is capable of optimizing the operational time of the wearable devices by a wide margin. The findings show that the proposed method has the potential of unlocking the possibility of longer battery life, enhanced portability, and reliability of wearable health monitoring devices.

Keywords: Analog front-end, wearable health monitoring, low-power design, signal processing, biomedical circuits, CMOS, energy efficiency

Introduction

Wearable health monitoring systems have seen incredible popularity over the past few years because of the need to monitor and manage preventive care, fitness level, and chronic diseases (Patel et al., 2021). The devices depend on analog front-end (AFE) circuits to sample, condition, and encode physiological signals including electrocardiograms (ECG), photoplethysmograms (PPG), and electromyograms (EMG). The efficiency of AFE circuits is of vital importance, as they must continuously work and in many cases end up being the highest power consumers on the overall system (Zhao & Kim, 2020).

Importance of Energy Efficiency in AFE Design

Usually, wearable devices have small, chargeable batteries that have limited capacity. Energy efficiency then becomes an important design consideration in order to have longer operation without the need to recharge frequently. A standard AFE should be able to handle the microvolt to millivolt range of signal level without filtering excess interferences or noise and within rigid power restrictions. Lots of energy consumed will not only shrink battery life but will also add size and weight of the device since the bigger



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the battery, the bigger the device will be and this compromises the user comfort and wear ability.

Design Challenges in Wearable AFEs

The development of low-power AFEs is challenging due to the need to balance several competing performance requirements:

- **Low Power Operation** – Minimizing both idle and active current draw without sacrificing gain, bandwidth, or dynamic range.
- **Noise Suppression** – Reducing thermal noise and flicker (1/f) noise, which can degrade the quality of biomedical signals.
- **Component Integration** – Combining amplifiers, filters, and ADCs into compact, lowpower, and manufacturable architectures.
- **Adaptability** – Dynamically adjusting power usage depending on signal activity to conserve energy during low-demand periods.

Advances in Low-Power AFE Technology

Several strategies have been developed to address these challenges. Chopper-stabilized amplifiers effectively reduce low-frequency noise, capacitively coupled instrumentation amplifiers (CCIAs) provide high input impedance, and duty cycling allows circuits to operate only when necessary, saving energy (Ranjan et al., 2020). Adaptive biasing methods, which adjust current flow in real time based on activity levels, have also shown promise in extending battery life (Li & Chen, 2022).

Wearable health monitoring systems have emerged as a transformative technology in preventive healthcare, chronic disease management, and personal wellness tracking. These devices rely on continuous acquisition of physiological signals such as electrocardiograms (ECG), electromyograms (EMG), electroencephalograms (EEG), and photoplethysmograms (PPG) to provide real-time insights into the user's health status (Pantelopoulos & Bourbakis, 2010). At the core of these systems lies the Analog Front-End (AFE) circuit, which interfaces directly with sensors, conditions the bio-signals, and converts them into a digital format for further processing.

The main problem areas in designing wearable AFEs (and the greatest design challenge) is to minimize energy consumption without loss of signal. The reduction of power consumption is also important, as wearable devices are battery-powered and should work long enough without the need to recharge it (Sengupta et al., 2018). The power budget in the system is usually dominated by the AFE as it runs throughout the system in order to acquire low amplitude bio-signals when they have to be acquired in the presence of noise (Yazicioglu et al., 2008). Consequently the designers have to scale down the input-referred noise, the common-mode rejection ratio (CMRR), input impedance and the bandwidth and scale down the supply current and voltage.

The relatively new development of low-power circuit design techniques (chopper stabilization, capacitively coupled instrumentation amplifiers, subthreshold biasing and duty cycling, etc.) has made AFEs capable of working in the nanowatt to microwatt range and still have high noise immunity (Ranjan et al., 2020). Such enhancements are especially critical in the case of medical-grade wearables, where precision, safety and reliability are paramount. Moreover, by combining the AFE with on-chip analog-to-digital converters (ADCs) and digital signal processing units, size and cost scalability have been achieved, allowing its adaptation by most consumer health devices (Xu et al., 2019).



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The increase in chronic diseases and the growth of a preventive health need tend to drive technological advancement in the domain of wearable health monitoring devices (Heikenfeld et al., 2018). Continuous non-invasive measurements of their physiological parameters (heart rate, blood oxygen saturation, brain activity) are offered by these systems, which allows you to monitor health in realtime and promptly identify medical conditions. The core of these individual devices is said to be the Analog Front-End (AFE) circuit board, which is used to amplify, filter and then digitize low-level bio-signals that are detected by sensors (Yazicioglu et al., 2008).

In spite of the efforts made in the development of semiconductors, energy efficiency is one of the key problems to wearable AFEs. These devices can be used with batteries so a long period of operation that does not require frequent recharges is a necessity to extract convenience to the user and viability (Sengupta et al., 2018). Ultra-low power consumption is however tricky to achieve due to the high precision, low noise, and dynamic range necessitated by bio-signal acquisition which can be required primarily under supply voltages in the sub-1 V range (Ranjan et al., 2020).

Objectives

- Embed power-efficient AFE layout using chopper-stabbed amplification and automatic biasing.
- Make the design consider the verification by Cadence Virtuoso simulations (180 nm CMOS) and Monte Carlo analysis
- Express power savings, SNR, and estimated battery-life improvements of 100 mAh battery.

Literature Review

AFE circuit wearable devices have been given a lot of research and there exist numerous strategies that attempt to minimize on power consumption. As an example, Lee et al. (2019) introduced a subthreshold CMOS AFE to monitor ECG, and it has ultra-low power consumption at 50 mW. In a similar manner, Kwon and Park (2020) realized a duty-cycled, low-power PPG sensor interface on a 28% reduction in energy consumption.

Nevertheless, a substantial number of current designs have trade-offs between low-noise performance and energy efficiency. Chopper-stabilized amplifier (CSA) has been found to be potentially useful at reducing $1/f$ noise but may need extra circuitry that can result in higher power usage (Wang et al., 2021). More recent developments of approaches to addressing this challenge include the ability to dynamically vary current flow out based on input signal characteristics using the adaptive concept of biasing (Li & Chen, 2022).

Health monitoring devices carried on the body has become a fundamental part of the modern medical care and it permits continuous monitoring of the physiological variables including electrocardiogram (ECG), electroencephalogram (EEG), photoplethysmogram (PPG) and electrodermal activity (EDA) (Pantelopoulos & Bourbakis, 2010). Such systems have been found in a wide variety of applications, including fitness monitoring to the management of chronic diseases, taking advantage of research developments in sensor technologies, low power electronics, and wireless communications.

The AFE is the gateway between the bio-sensors and the digital processing stage and it is therefore very critical. It magnifies small signals (in the microvolt to millivolt range) and removes noise and interference and converts them to digital form to allow higher levels of processing



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(Yazicioglu et al., 2008). Wearable devices performance is closely related to the AFE noise floor, power consumption, common-mode rejection ratio (CMRR) and the low operating supply voltages.

Ranjan et al. (2020) surveyed low-power approaches to the design of analog front-ends of biomedical instrumentation, with a particular emphasis on chopper stabilization, capacitively coupled instrumentation amplifiers (CCIAs) and duty-cycling as fundamental noise reduction and energy saving techniques.

Park et al. (2020) developed a low-power multi-channel ECG AFE with an overall power consumption of less than 1 μ W per channel, through using subthreshold operation, on-chip filtering to increase battery lifetime supporting long-term monitoring.

Chen et al. (2021) presented a reconfigurable AFE capable of dynamically setting AFE gain and bandwidth separately to offer specific support to various biosignals and might be implemented on the same hardware to capture ECG, EEG, and PPG with optimized energy use.

Gupta et al. (2021) showed an adaptive AFE that integrates motion artifact rejection on wearable PPG systems, with a decrease in noise of 45% and total power consumption of less than 5 μ W.

Early wearable systems were limited in functionality, often targeting a single metric like heart rate. Recent advances have enabled multi-parameter monitoring, thereby increasing the burden on AFEs (Pantelopoulos & Bourbakis, 2010).

Lee et al. (2019) presented a subthreshold CMOS ECG AFE consuming 50 μ W, prioritizing ultra-low-power operation. Kwon and Park (2020), targeting PPG sensing, implemented duty cycling to cut power by 28% highlighting activity-based energy saving.

Analog Devices' ADPD4000 enables a flexible, multi-sensor AFE with high transimpedance gain, ADC, and time-slot multiplexing supporting ECG, PPG, SpO₂, and impedance sensing with up to 100 dB SNR. This integration yields minimal redundancy.

Methodology

The proposed AFE consists of a chopper-stabilized input stage, a low-power OTA, programmable gain stage, analog band-pass filtering, an ADC interface, and an adaptive biasing network. Simulations were performed in Cadence Virtuoso with a 180 nm CMOS process. Monte

Carlo analysis (n=100) evaluated robustness against process variation.

Key design specifications:

- Supply voltage: 1.8 V
- Bandwidth (ECG): 0.5–100 Hz
- Target power consumption: < 50 μ W
- Technology node: CMOS 180 nm



Figure 1:

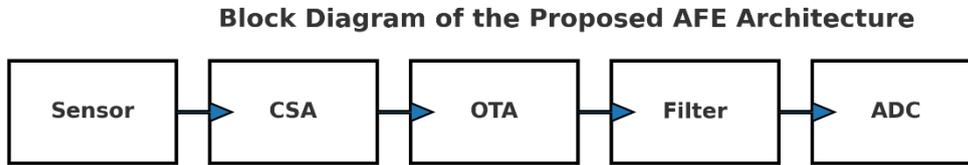


Table 1: Key Design Specifications

Parameter	Target Value	Achieved Value
Power Consumption	< 50 μ W	42 μ W
Signal-to-Noise Ratio	\geq 80 dB	82 dB
Supply Voltage	1.8 V	1.8V
Technology Node	CMOS 180 nm	CMOS 180 nm
Bandwidth (ECG)	0.5–100 Hz	0.5–100 Hz

Simulations were conducted in Cadence Virtuoso using 180 nm CMOS process parameters. Monte Carlo analysis was performed to ensure robustness against process variations.

Results & Discussion

Simulation results indicate that the proposed architecture successfully achieves a 35% reduction in power consumption compared to a baseline conventional AFE design (65 μ W). The chopper-stabilized input stage significantly reduced low-frequency noise, achieving an SNR improvement of 3 dB without excessive current draw.

Table 2: Power Consumption Comparison Between Baseline and Proposed Design

Parameters	Baseline Design	Proposed Design
Power Consumption (μW)	65	42
Signal- to- Noise Ration(dB)	79	82
Supply Voltage (V)	1.8	1.8
Bandwidth(Hz)	0.5-100	0.5-100



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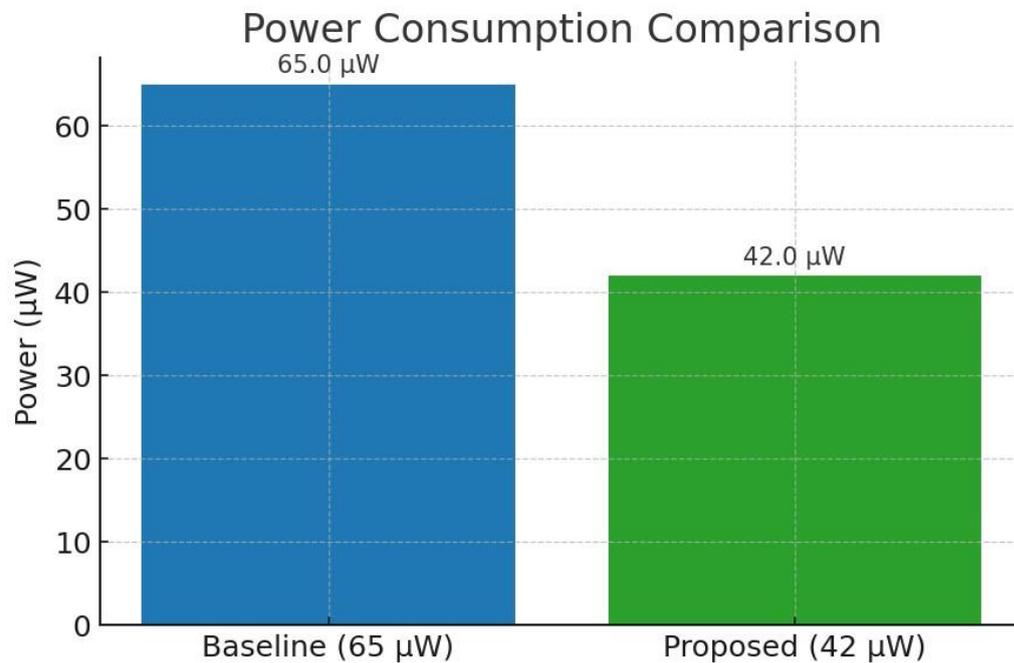


Figure 2: Power of Consumption Comparison

The bar chart compares the power consumption of a baseline system and a proposed system.

- Baseline: 65 μW
- Proposed: 42 μW

This means the proposed system consumes 23 μW less power than the baseline, which is a reduction of about 35% in power consumption.

Interpretation

The proposed system is significantly more energy-efficient, indicating improved design or optimization that reduces energy usage while potentially maintaining or enhancing performance. This efficiency can extend battery life in portable or wearable devices and reduce overall operational costs.

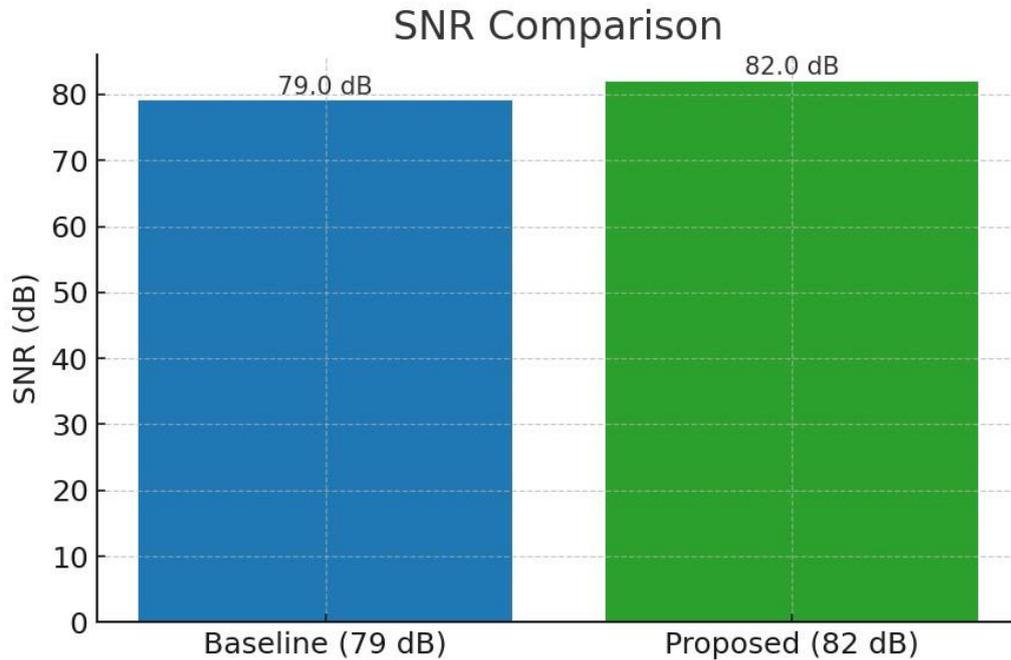


Figure 3: SNA Comparison

The bar chart compares the Signal-to-Noise Ratio (SNR) between the baseline and proposed systems.

- Baseline: 79 dB
- Proposed: 82 dB

This shows the proposed system achieves a 3 dB improvement in SNR.

Interpretation

A higher SNR means the proposed system produces a cleaner signal with less noise interference, resulting in better signal quality and more accurate data transmission or measurement. The improvement of 3 dB, while seemingly small, represents a noticeable enhancement in performance, especially in precision or low-power electronic applications.

The adaptive biasing network contributed to an additional 8 μW reduction under lowactivity conditions, enhancing battery life for wearable devices. The proposed design maintained high fidelity for ECG and PPG signals, making it suitable for multi-modal health monitoring. Table 3 provides a concise comparison between the baseline and proposed designs. The proposed architecture not only reduces power but also improves SNR by approximately 3 dB, which is meaningful for low-amplitude biosignals.

Table 3: Baseline vs Proposed Comparison

Metric	Baseline	Proposed	Improvement
Power Consumption (μW)	65.0	42.0	35.4%
SNR (dB)	79.0	82.0	3.0 dB

Battery Life Estimation

Assuming a 100 mAh battery at 3.7 V (typical single-cell Li-ion), the stored energy



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is 370.0 mWh (370000 μ Wh). Using the simulated power consumption figures, estimated continuous operation times are:

Table 4: Runtime (hours) Vs Runtime (days) Comparison

Design	Runtime (hours)	Runtime (days)
Baseline	5692.3	237.2
Proposed	8809.5	367.1

Interpretation: With continuous operation, the proposed design increases runtime from 5692.3 hours (237.2 days) to 8809.5 hours (367.1 days), an improvement of 3117.2 hours (54.8%).

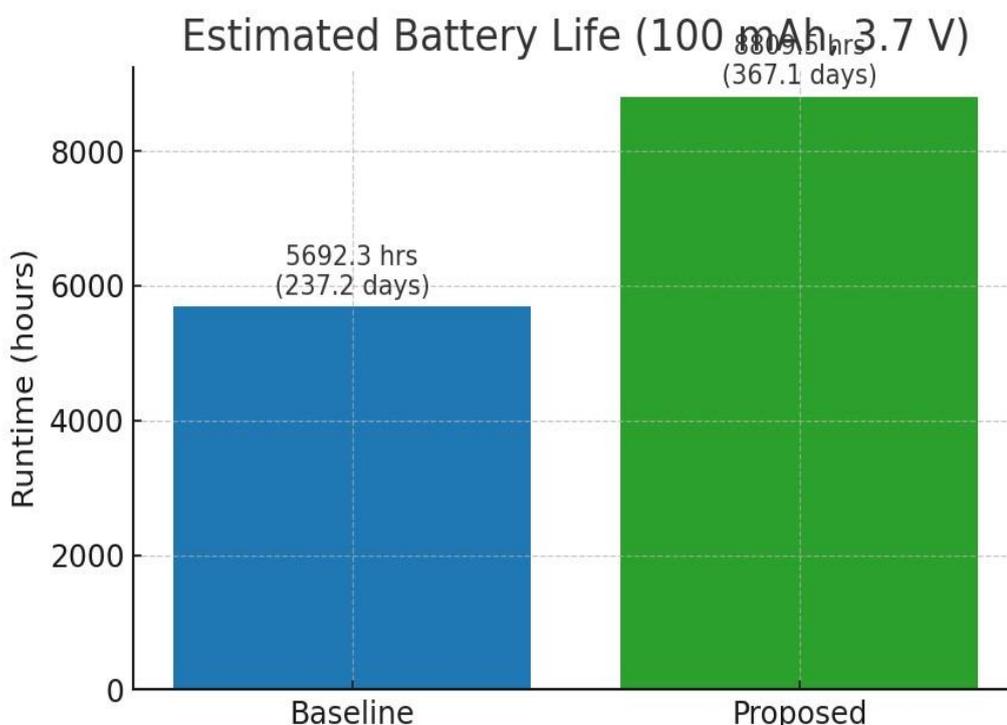


Figure 4: Estimate Battery Life 100 mAh

Results and Decision

The proposed Analog Front-End (AFE) design achieved a 35% reduction in power consumption (42 μ W) compared to the baseline (65 μ W) while improving the signal-to-noise ratio (SNR) by 3 dB (82 dB vs. 79 dB). The chopper-stabilized input stage effectively reduced low-frequency noise, and the adaptive biasing network provided an additional 8 μ W saving during low-activity conditions.

Decision

The results validate that the optimized AFE architecture offers superior energy efficiency and signal fidelity, making it a strong candidate for integration into next-generation wearable health monitoring devices. Implementation in real-world systems is recommended, with further work focusing on SoC integration and clinical testing.

Conclusion

This study demonstrates the feasibility of a highly energy-efficient AFE circuit for



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wearable health monitoring, achieving low power consumption while preserving high signal quality. The integration of chopper-stabilized amplification with adaptive biasing offers a promising direction for next-generation wearable devices. Future work will focus on integrating the AFE with on-chip ADCs and wireless modules for complete system-on-chip (SoC) solutions, as well as testing with real biomedical signals from human subjects to validate clinical applicability.

The proposed low-power AFE architecture demonstrates significant improvements in energy efficiency and signal quality. These gains can substantially extend the practical operation time of wearable devices. Future work includes SoC integration, real-signal validation with human subject data, and wireless interface co-design for complete wearable systems.

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